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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/204,585
Filing Date: December 03, 1998
Appellant(s): TREMBLAY ET AL.

DAVID W. O'BRIAN
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed august 24, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because the expression $N_G + (M * N_L)$ for the total number of registers and the statement "the number of address bits for addressing the entire $N_G + (M * N_L)$ registers being equal to the number of bits B that are used to address $N = 2^B$ registers" appear to be incorrect.

The support of independent claims 1, 15 and 23 is shown in Figure 6 and is originally described in the first paragraph appeared on page 18 of the specification. The paragraph is substituted by an amendment (amendment D1) filed on March 28, 2003.

With respect to independent claims 1, 15 and 23, Figure 6 shows a processor comprising a decoder, a plurality of register file segments (61X) and a plurality (M units) of functional units (62X). Each of the register file segments is associated with a functional unit (therefore, there are M pieces of register file segments). In the claimed invention, each of the register file segments is further partitioned into global registers (N_G) and local registers (N_L). The local registers are accessible only by the functional unit associated with the register file segment containing the local registers. All the global register segments are shared by all the functional units.

The support for claims 8, 21 and 28 can be found in Figure 6 and in line 17 of page 18 to line 6 of page 20 of the specification.

With respect to claims 8, 21 and 28, the expression $N_G + (M * N_L)$ for the total registers (the entire register file before it is partitioned into M pieces) available for the M functional units appears to be incorrect because there are M, and not one as shown in the expression, pieces of N_G. The correct expression appears to be $M * (N_G + N_L)$, with M represents total number of segments or total number of functional units, N_G represents the number of global registers in a single register file segment (616 for example) and N_L represents the number of local registers in a single register file segment.

The expression $N = N_G + N_L$ for the total number of registers in a single file segment (616 for example) is correct.

Appellants' statement "the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits that are used to address $N = 2^B$ registers" appears to be incorrect because it is impossible to use 2^B addresses to access the entire register file because either $M * (N_G + N_L)$ or $N_G + (M * N_L) > 2^B$. In other words, there are more registers than available addresses to address them.

The errors appear to be inadvertent because they are mathematic and not technical errors.

(6) Issues

The appellant's statement of the issues in the brief is incorrect. The correct issues are as follows:

a. Whether claims 1, 3-14 and 23-28 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Laun,

b. Whether claims 2, 15-22 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Yung and Laun further in view of Nashimoto,

c. whether claims 1, 3-14 and 23-28 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Laun and

d. whether claims 2, 15-22 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Laun in view of Nashimoto.

In the interest of simplifying issues for appeal, rejections represented by c and d above are withdrawn.

(7) Grouping of Claims

The appellant's statement in the Brief that certain claims do not stand or fall together is not agreed with because 1. Appellants do not contest the use of Nishimoto as disclosure of a decoder for decoding VLIW instructions and 2. there is no separate argument provided for each of the rejected claims 2-7, 9-20 and 22-27. Claims 1-28 are therefore grouped as follow:

Group 1: 1-7, 9-20 and 22-27, all claims within this group stand or fall with claim 1 because there is no separate argument presented by Appellants for each of the other claims.

Group 2: There is no claim in this group because Appellants agree with the Examiner on the teaching of Nashimoto. The original claims in this Group are merged with Group 1.

Group 3: 8, 21 and 28, all claims within this group stand or fall with claim 8 because there is no separate argument presented by Appellants for each of the other claims.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,592,679	Yung	1-1997
5,911,149	Luan	6-1999
6,023,757	Nishimoto	2-2000

(10) Grounds of Rejection

In the interest of simplifying issues on appeal, the rejections of

c. claims 1, 3-14 and 23-28 under 35 U.S.C. 103(a) over Laun, and

d. claims 2, 15-22 under 35 U.S.C. 103(a) over Laun in view of Nashimoto

are hereby withdrawn.

The following ground(s) of rejection are applicable to the appealed claims:

a. Claims 1, 3-14 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Laun,

With respect to independent claim 1 (Group 1), Yung taught:

1. A processor (200, Figure 2 and lines 37-38 of column 4), comprising:

a plurality of functional units (execution pipes 241, 242, 24X, etc. Figure 2); and

a register file (register file 135 of Figure 1) that is divided (Please see the last paragraph in the BACKGROUND OF THE INVENTION on column 2. The thrust of Yung's invention is to divide the prior art register file 135, Figure 2, into pieces, one for each execution pipe, as shown in Figure 2.) into a plurality of register file segments (local register buffer 241d, 242d, 24Xd, etc and global register file 290 in Yung), each

coupled to and associated with respective ones of the plurality of functional units (execution pipes 241, 242 and 24X etc. in Figure 2 of Yung), the register file segments each implemented as an addressable array and partitionable into global registers and local registers (the global register is separated from the local register buffers), the global registers being accessible by the plurality of functional units (global register file is shown in Figure 2 of Yung to be connected to and accessed by all the execution pipes), the local registers being accessible by the functional unit associated with the register file segment containing the local registers (the drawing shows that each of the local register buffers is respectively associated with an execution pipe), wherein the number of global registers and the number of local registers are programmably configurable (the teaching of the secondary reference, Luan).

The only difference is that the number of global registers and the number of local registers within a segment do not appear to be programmably configurable as recited in the wherein clause. Programmably configurable memory is well known in the art. Attention of the Board is respectfully directed to lines 1-6 of the abstract in Luan. Luan teaches a memory system and an apparatus for programmably partitioning a portion of the memory to be used by a processor and the other portion to be shared by the processor and a peripheral device. Since both references are directed toward partitioning memory, it would have been obvious to a person of ordinary skill in the art to incorporate a programmably configurable memory as taught by Luan in Yung such that the sizes of the local register buffer and the global register are programmably configurable.

Claims 3-14 and 23-28 stand or fall together with claim 1 because there are no separate arguments presented for the claims.

Claims 8, 21 and 28 (group 3) recite that:

A. there are M register file segments (because there are M function units with one register file segment for each M functional units),

B. each of the register file segments has N physical registers and is partitioned into a local register file which has N_L physical registers and a global register file which has N_G physical registers => $N_L + N_G = N$,

C. the register file having $N_G + (M * N_L)$ total registers available for the M functional units,

D. the number of address bits for addressing the entire $N_G + (M * N_L)$ registers being equal to the number of bits B that are used to address $N = 2^B$ registers.

Items A above merely recites that the number of segments is equal to the number of functional units. Yung meets this limitation because Yung requires associating each one of the execution pipes with a local register buffer. The number of segments therefore is equal to the number of functional units in Yung.

Item B above recites (1) that each of the M segments has a portion of local registers and a portion of global registers and (2) that the letter N represents the sum of local registers and global registers within a segment. With respect to (2), this is mere a mathematical relationship between the partitions and the total before it is partitioned. It is a mathematical fact that the sum of the partitions is always equal to the total. With respect to (1) above, Yung also has M segments (local register buffer 241d, 24Xd, etc.)

and each of the segments is associated with an execution pipes (Figure 2). The only difference is that the global register file of Yung is shown as 1 piece whereas Appellants' global register file is divided into M pieces. It is noted that dividing the global register file into M pieces has no practical or functional value. The practical or functional value of the global register file is that all the execution pipes are allowed to access all the global registers. Yung meets this limitation. Whether the global memory is in one piece or M pieces is a matter of design choice because in either case it does not affect the functionality of the global register file, namely, access by all the functional units. The global register of Yung is shown as one piece instead of M pieces to reflect the fact that it is shared by all the execution pipes. Given the teaching of Luan that a memory is programmably partitionable, it would have been obvious to a person of ordinary skill in the art to programmably partition a memory in any manner, one piece or M pieces for example, he likes.

With respect to C above, as discussed in the Summary of The Invention above, the expression $N_G + (M * N_L)$ expressing the total number of registers in the register file appears to be incorrect if the global memory is divided into M pieces. If the global register file is divided into M pieces, the correct expression is $M * (N_G + N_L)$. However, if the global register is in one piece as taught by Yung instead of M pieces, the expression $N_G + (M * N_L)$ in claims 8, 21 and 28 expressing the total number of registers in the register file then is correct. The expression as currently appeared in claims 8, 21 and 28 suggests that Appellants' global register file actually is in one piece as Yung and not in M pieces. In anyway, the expression mere expresses the total number of registers in

the register file and have no practical or functional values. In either case, all the functional units are able to share the global registers.

With respect to D above, as discussed in the Summary of The Invention above, it appears that it is impossible to address the entire register file with the number of addresses for one segment. For example, for a register file having 64 registers, it requires 6 bit address (2^6 = 64). If the register file is divided into 4 pieces with 16 registers each, the register piece requires 4 bit address (2^4 = 16). A 4 bit address can only address 16 registers and not 64 registers.

In anyway, it is well known that the number of address bits for 2^b registers is always b.

Claims 21 and 28 stand or fall with claim 8 because there are no separate arguments presented for the calims.

b. Claims 2, 15-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, Laun and further in view of Nashimoto.

This rejection is set forth in a prior Office Action, mailed on 5/1/2002 (paper #17). Appellants agree with the Examiner on the teaching of Nashimoto (lines 1-2 of page 7 and lines 15-16 of page 11 of the Brief).

(11) Response to Argument

The Examiner acknowledges Appellants' ground of appeal set forth on pages 5-8 of their Brief. The Examiner disagrees with Appellants' statement that no *prima facie* case of obviousness has been made out.

Group 1

With respect to Appellants' arguments in Group 1 (pages 8-11), Appellants rely on the claim language "***register file segments each coupled to, and associated with, a respective functional unit and each implemented as an addressable array and partitionable into global and local registers***" for patentability. The thrust of the instant invention is to decentralize, partition or divide a central register file into segments and to respectively associate selected segments to a plurality of functional units in a processor having a plurality of functional units. This is exactly the teaching of Yuan. Attention of the Board is respectfully directed to the last paragraph in the BACKGROUND OF THE INVENTION in column 2 of Yung.

Attention of the Board is further respectfully directed to Figures 1 and 2 in Yuan. Figure 1 of Yuan shows a prior art processor having a centralized register file 135 and 190, and a plurality of execution units 14X (or functional units). Figure 2 of Yuan shows an improvement of the prior art processor. Yuan's teaching or the improvement is to decentralize, partition or divide the central register file shown in Figure 1 into segments as shown in Figure 2. Figure 2 shows that the central register file is partitioned into segments such as global register file 290 and local register 241d, 242d, 24Xd etc. one for each execution pipe. The global register file 290 is shown as one piece in Yung because it is shared or accessible by all the functional units. Further dividing the global register files into pieces does not serve any purpose. In both Appellants' and Yung's inventions, all the global registers are shared regardless of how many pieces the global register file is divided. Furthermore, there is no need to associate any piece of global

register segment to a functional unit (the last sentence on page 8 of the Brief) because the global registers are shared by and not dedicated to any functional units. The dividing of global register file amounts to design choice and is not patentable distinct over Yung. There is no explanation by Appellants as to why dividing the shared global register file is patentable distinct over Yung. Further, Appellants' expression $N_G + (M * N_L)$ suggests that the global register file is in one piece and not M pieces.

As to the argument of ***the number of local registers and the number of global registers in Yung is not programmably configurable*** (see the second paragraph of page 9 of the Brief and the last paragraph on page 10), that is the teaching of the second reference, Luan. Yung taught decentralize or partition a register file (135 in Figure 1) into segments (24Xd, Figure 2). Yung does not make clear whether partition is implemented by programmable configuration. Laun taught a computer system which has a programmable shared memory system that selectively dedicates (programmablly configurable) a first portion of memory to use by the processor and allocates a second portion of memory to share use by the processor and any peripherals in the system (the abstract of Laun). Since both Yung and Laun taught partitioning memory or register, it would have been obvious to a person of ordinary skill in the art to partition Yung's register file programmably such that the size of the partitions can programmably be varied.

As to Appellants' argument that memory and register are different and Laun taught programmably partitioning memory therefore is different from partitioning register and therefore is patentable. The Examiner disagrees. Register is a sub-set of memory

because memory is made up of registers and they both are for storing information represented by 0 and 1. The term register is used in the computer art to represents those memories used by an ALU because they are smaller in size and usually for storing operands. Programmably partitioning a memory is no different than programmably partitioning a register file. They both involve selectively coupling memory banks or register sets to a bus, in the case of Yuan, selectively coupling register set or memory bank to respective execution pipe buses. It is inherent that the address ranges or address spaces have to be redefined because otherwise it does not work. Appellants fail to explain why and how programmably partitioning a memory is different than programmably partitioning a register file.

Group 2

With respect to the arguments in Group 2, claims 15-20 and 22 are in Group 2 because they recite VLIW. The Nishimoto reference is recited for that feature. Appellants agree with the Examiner on the teaching of Nishimoto and therefore do not contest the rejection. In Group 2, Appellants rely on the same limitations as Group 1 for patentability. The Examiner's response in Group 1 therefore is incorporated herein by reference thereto.

Group 3

Appellants' arguments in Group 3 have already been response to by the Examiner in the Rejections and the Summary of The Invention above. The response is

incorporated herein by reference thereto. Further, Appellants fail to explain why and how the recitations are patentable and distinct over Yung in view of Luan, let alone they are erroneous.

IN CONCLUSION

Same as Yung's invention, the thrust of the instant invention is to decentralize a central register file. It is a matter of design choice as to how many pieces a global register file is partitioned. It would have been obvious to a person of ordinary skill in the art to programmably partition a register segments into local register segment and global register segment as taught by Laun so that the number of register in the local segment and the global segment are variable. Appellants did not provide any arguments as to why the mathematic expressions are patentable distinct over Yung.

For the above reasons, it is believed that the propriety of the rejections remains intact. It is therefore respectfully requested that the rejections be sustained.

Respectfully submitted,

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Primary Examiner
November 6, 2004

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